In re Patent Application of
COFLER ET AL.
Serial No. **10/082,816**
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In the Claims:

This listing of claims replaces all prior versions and listings of claims in the application.

Claims 1-24 (Canceled).

25. (Currently amended) A method of handling branching instructions using a processor comprising a program memory storing program instructions, and a processor core comprising a plurality of processing units and a central unit connected thereto, the processing units comprising a first processing unit including at least one address-pointing register, the central unit issuing instructions to the processing units based upon the program instructions, the method comprising:

clocking the processor core with a clock signal;

receiving a branching instruction in the course of a current clock cycle, the branching instruction using a content of the at least one address-pointing register; ~~and~~

executing the received branching instruction in the course of the current clock cycle; and

checking validity of the content of the at least one address-pointing register at a start of the current clock cycle so that the branching instruction is received by the central unit and executed if the content is declared valid, and, in an opposite case, the branching instruction is kept on hold for executing until the content is declared valid.